UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/770,571	01/26/2001	Ahmad Tawil	016295.0635	7613

7590 06/16/2005

Khannan Suntharam
Baker Botts L.L.P.
One Shell Plaza
910 Louisiana Street
Houston, TX 77002-4995

EXAMINER	
LEE, PHILIP C	
ART UNIT	**PAPER NUMBER**
2154	

DATE MAILED: 06/16/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/770,571	TAWIL ET AL.	
	Examiner	Art Unit	
	Philip C. Lee	2154	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 October 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☒ Interview Summary (PTO-413) Paper No(s)/Mail Date. 6/9/05
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. This is a supplemental office action to correct an improper final rejection on claims 23-34, mailed on 4/5/05.

2. Applicant's arguments with respect to claims 1-22, filed 10/18/04, have been fully considered but are moot in view of new grounds of rejection. Applicant's arguments with respect to claims 23-34, filed 10/18/04, have been fully considered but are not deemed to be persuasive.

Claim Rejections – 35 USC 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3 and 5-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunlock, U.S. Patent 6,606,630 (hereinafter Gunlock) in view of Schatzberg, U.S. Patent 6,615,284 (hereinafter Schatzberg).

5. Gunlock was cited in the last office action.

6. As per claim 1, Gunlock taught the invention substantially as claimed comprising:

a high speed network interconnect (col. 6, lines 17-26; fig. 1) ;

one or more target devices coupled to the high speed network interconnect, wherein each target device has a unique hardware address (fig. 1; col. 6, lines 17-26; col. 8, lines 13-25);

a host, wherein the host comprises a host bus adapter operable to perform a port login with a target device (col. 4, lines 58-63; col. 6, lines 32-48; col. 8, lines 25-27); and

a unique hardware address table stored in a memory (col. 6, lines 40-43), wherein the unique hardware address table stores the unique hardware address of every target device (col. 9, lines 54-62; col. 8, lines 13-27).

7. Gunlock did not teach not attempting to perform a port login with a target device unless the unique hardware address of that target device is present on the unique hardware address table. Schatzberg taught a similar system wherein a unique hardware address table stored in a memory location associated with the host bus adapter, wherein the unique hardware address table stores the unique hardware address of every target device that the host is authorized to access such that the host bus adapter will not attempt to perform a port login with a target device unless the unique hardware address of that target device is present on the unique hardware address table (col. 4, lines 52-55; col. 5, lines 17-24, 43-63).

8. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock and Schatzberg because Schatzberg's teaching of a unique hardware address table in the host bus adapter would simplify the complexity of the disk controller's design in Gunlock's system by allowing the function of the already complex disk controller software to be implemented by the bus controller (col. 5, lines 47-53).

9. As per claim 2, Gunlock and Schatzberg taught the invention substantially as claimed in claim 1 above. Gunlock further taught wherein the unique hardware address is a port name (col. 8, lines 21-25).

10. As per claim 3, Gunlock and Schatzberg taught the invention substantially as claimed in claims 1 above. Gunlock further taught wherein the unique hardware address is a node name (col. 8, lines 21-25).

11. As per claim 5, Gunlock and Schatzberg taught the invention substantially as claimed in claim 1 above. Gunlock further taught wherein the target device is a storage device (col. 6, lines 17-24; col. 7, lines 19-20).

12. As per claim 6, Gunlock and Schatzberg taught the invention substantially as claimed in claim 1 above. Gunlock further taught wherein the HBA comprises the memory (col. 6, lines 40-43).

13. As per claims 7 and 8, Gunlock and Schatzberg taught the invention substantially as claimed in claim 1 above. Gunlock further taught wherein the high speed network interconnect is a high speed optical network interconnect (col. 6, lines 17-21).

14. Claims 23-25, 27-31 and 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunlock in view of Saegusa, U.S. Patent 6,745,281 (hereinafter Saegusa).

15. Saegusa was cited in the last office action.

16. As per claims 23 and 29, Gunlock taught the invention substantially as claimed comprising:

a memory (col. 6, lines 40-43);

a unique hardware address table stored in a memory (col. 6, lines 40-43), operable to contain one or more unique hardware address corresponding to one or more target device (col. 9, lines 54-62; col. 8, lines 13-27).

17. Gunlock did not teach not performing a port login with a target device unless the unique hardware address is present on the unique hardware address table. Saegusa taught the host is authorized to access such that the HBA will not perform a port login with a target device unless

the unique hardware address of that target device is present on the unique hardware address table (col. 14, lines 1-45; col. 11, lines 51-57).

18. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock and Saegusa because Saegusa's teaching of authorized access table would increase the security of Gunlock's system by allowing only the authorized host to access the target devices.

19. As per claims 24 and 30, Gunlock and Saegusa taught the invention substantially as claimed in claims 23 and 29 above. Gunlock further taught wherein the unique hardware address is a port name (col. 8, lines 21-25).

20. As per claims 25 and 31, Gunlock and Saegusa taught the invention substantially as claimed in claims 23 and 29 above. Gunlock further taught wherein the unique hardware address is a node name (col. 8, lines 21-25).

21. As per claims 27 and 33, Gunlock and Saegusa taught the invention substantially as claimed in claims 23 and 29 above. Gunlock further taught wherein the target device is a storage device (col. 6, lines 17-24; col. 7, lines 19-20).

22. As per claims 28 and 34, Gunlock and Saegusa taught the invention substantially as claimed in claims 1, 23 and 29 above. Gunlock further taught wherein the HBA comprises the memory (col. 6, lines 40-43).

23. Claims 4 and 9-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunlock and Schatzberg in view of Blumenau et al, U.S. Patent 6,665,714 (hereinafter Blumenau).

24. Blumenau was cited in the last office action.

25. As per claim 4, Gunlock and Schatzberg taught the invention substantially as claimed in claim 1 above. Gunlock and Schatzberg did not teach using a World-Wide Name. Blumenau taught wherein the unique hardware address is a World-Wide Name (col. 6, lines 65-67; col. 22, lines 4-11).

26. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock, Schatzberg and Blumenau because Blumenau's teaching of World-Wide Name would enhance Gunlock's and Schatzberg's systems by providing a unique identification for identifying each storage device (col. 22, lines 7-11).

27. As per claim 9, Gunlock taught the invention substantially as claimed for managing the port login performed by a host bus adapter for a host that is communicatively coupled to a fabric,

wherein one or more target devices, each having a unique hardware address, are coupled to the fabric (fig. 1, lines 17-26; col. 8, lines 13-25) comprising:

determining whether the unique hardware address of an available target device is present on a unique hardware address table, wherein the unique hardware address table contains the unique hardware addresses of each target device (col. 8, lines 13-27).

28. Gunlock did not teach performing a port login based on the unique hardware address table. Schatzberg taught a similar system wherein a unique hardware address table stored in a memory location associated with the host bus adapter, wherein the unique hardware address table contains the unique hardware addresses of each target device that the host is authorized to access; and performing a port login with each target device whose unique hardware address is present on the unique hardware address table (col. 4, lines 52-55; col. 5, lines 17-24, 43-63).

29. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock and Schatzberg because Schatzberg's teaching of a unique hardware address table in the host bus adapter would simplify the complexity of the disk controller's design in Gunlock's system by allowing the function of the already complex disk controller software to be implemented by the bus controller (col. 5, lines 47-53).

30. Gunlock and Schatzberg did not teach querying for available target devices. Blumenau taught from the host bus adapter, querying the fabric for available target devices and receiving at

the host bus adapter an identification of available target devices (col. 6, lines 62-col. 7, line 12; col. 8, lines 35-36; col. 21, lines 67-col. 22, lines 14).

31. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock, Schatzberg and Blumenau because Blumenau's method of querying the fabric for available target devices would increase the efficiency of Gunlock's and Schatzberg's systems by avoiding login attempt to unavailable target devices by the host.

32. As per claim 16, Gunlock taught the invention substantially as claimed for managing a port login performed by a host bus adapter for a host that is communicatively coupled to a fabric, wherein one or more target devices, each having a unique hardware address, are coupled to the fabric (fig. 1, lines 17-26; col. 8, lines 13-25); comprising the steps of:

storing the unique hardware address of the selected target devices to a unique hardware address access table (col. 4, lines 58-63; col. 6, lines 40-43; col. 8, lines 13-25).

33. Gunlock did not teach selecting target devices and not performing a port login with a target device unless the unique hardware address is present on the unique hardware address table. Schatzberg taught selecting target devices that may be accessed by the host and storing the unique hardware address of the selected target devices to a unique hardware address access table, wherein the host bus adapter will not perform a port login with a target device unless the unique

hardware address of that target device is present on the unique hardware address table (col. 4, lines 52-55; col. 5, lines 17-24, 43-63).

34. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock and Schatzberg because Schatzberg's teaching of a unique hardware address table in the host bus adapter would simplify the complexity of the disk controller's design in Gunlock's system by allowing the function of the already complex disk controller software to be implemented by the bus controller (col. 5, lines 47-53).

35. Gunlock and Schatzberg did not teach querying for available target devices. Blumenau taught from the host bus adapter, querying the fabric for available target devices and receiving at the host bus adapter an identification of available target devices (col. 6, lines 62-col. 7, line 12; col. 8, lines 35-36; col. 21, lines 67-col. 22, lines 14).

36. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock, Schatzberg and Blumenau because Blumenau's method of querying the fabric for available target devices would increase the efficiency of Gunlock's and Schatzberg's systems by avoiding login attempt to unavailable target devices by the host.

37. As per claims 10 and 17, Gunlock, Schatzberg and Blumenau taught the invention substantially as claimed in claims 9 and 16 above. Gunlock further taught wherein the unique hardware address is a port name (col. 8, lines 21-25).

38. As per claims 11 and 18, Gunlock, Schatzberg and Blumenau taught the invention substantially as claimed in claims 9 and 16 above. Gunlock further taught wherein the unique hardware address is a node name (col. 8, lines 21-25).

39. As per claims 12 and 19, Gunlock, Schatzberg and Blumenau taught the invention substantially as claimed in claims 9 and 16 above. Blumenau further taught wherein the unique hardware address is a World-Wide Name (col. 6, lines 65-67; col. 22, lines 4-11).

40. As per claims 13 and 20, Gunlock, Schatzberg and Blumenau taught the invention substantially as claimed in claims 9 and 16 above. Gunlock further taught wherein the target device is a storage device (col. 6, lines 17-24; col. 7, lines 19-20).

41. As per claims 14 and 21, Gunlock, Schatzberg and Blumenau taught the invention substantially as claimed in claims 9 and 16 above. Gunlock further taught wherein the HBA comprises the memory (col. 6, lines 40-43).

42. As per claims 15 and 22, Gunlock, Schatzberg and Blumenau taught the invention substantially as claimed in claims 9 and 16 above. Gunlock further taught wherein the high speed network interconnect is a high speed optical network interconnect (col. 6, lines 17-21).

43. Claims 26 and 32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Gunlock and Saegusa in view of Blumenau.

44. Blumenau was cited in the last office action.

45. As per claims 26 and 32, Gunlock and Saegusa taught the invention substantially as claimed in claims 23 and 29 above. Gunlock and Saegusa did not teach using a World-Wide Name. Blumenau taught wherein the unique hardware address is a World-Wide Name (col. 6, lines 65-67; col. 22, lines 4-11).

46. It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Gunlock, Saegusa and Blumenau because Blumenau's teaching of World-Wide Name would enhance Gunlock's and Saegusa's systems by providing a unique identification for identifying each storage device (col. 22, lines 7-11).

47. In the remark applicant argued that

(1) Seagusa does not teach a hardware address table stored in a memory location associated with the host bus adapter as in claims 23 and 29.

(2) cited references do not teach a host bus adapter having a memory for storing a hardware address table that includes a listing of target devices with which the host bus adapter is authorized to perform a port login as in claims 23 and 29.

48. In response to points (1) and (2), Gunlock taught a unique hardware address table stored in a memory associated with the host bus adapter (col. 6, lines 40-43). Gunlock did not teach not performing a port login with a target device unless the unique hardware address is present on the unique hardware address table. Saegusa taught a hardware address table including listing of target devices with which is authorized to perform a port login (col. 14, lines 1-45; col. 11, lines 51-57). This means Gunlock and Saegusa, in combination, taught a host bus adapter having a memory for storing a hardware address table that includes a listing of target devices with which the host bust adapter is authorized to perform a port login.

49. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

50. A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however,

will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action. Any inquiry concerning this communication or earlier communications form the examiner should be directed to Philip Lee whose telephone number is (571) 272-3967. Any inquiry of a general nature or relating to the status of this application should be directed to the Group receptionist whose telephone number is (703) 305-9600.

Philip Lee

JOHN FOLLANSBEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100